REMARKS/ARGUMENTS

Claims 1-9 and 18-20 are canceled without prejudice. Claims 10-17 remain pending in this application and stand rejected. Claims 1-3, 8-9, and 20 stand rejected under 35 U.S.C. § 101 as being non-statutory for failing to produce any real world tangible result. Claims 1-3, 8-9 and 18 further stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kerns el al., U.S. Patent 6,819,679, (hereinafter Kerns), Sakalian et al. (U.S. Patent No. 5,056,119, hereinafter Sakalian) in view of Koyama (U.S. Patent No. 6,047,04 hereinafter Koyama).

Claims 4-7 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kerns, Sakalian, Koyama, in view of Wright et al. (U.S. Patent No. 7,103,049, hereinafter Wright). Claim 19 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Kerns, Sakalian, Koyama, in view of Mo et al. (U.S. Patent No. 7,151,773, hereinafter Mo). Claim 20 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Kerns, Sakalian, Koyama, in view of Taborek, Sr. et al. (US 7,020, 729, hereinafter Taborek). Claims 10, 13-16, and 17 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Taborek, and further in view of Claims 11-12 stand rejected under Taborek, Wright, and further in view of Swoboda et al. (US Patent No. 6,085,336, hereinafter Swoboda). Claims 1-9 and 18-20 are canceled above thus rendering their rejections moot.

Claim 10 has been amended to more clearly define the scope of the invention recited therein. Support for the amendment to claim 10 is provided, for example, in paragraphs [0029] - [0031], reproduced below for the Examiner's convenience.

> "[0029] The parallel outputs of the S/P converter 303 are coupled to a first register 301 which is also 128 bits wide. For every 128 bits of the input serial data stream D(i) that is shifted into the S/P converter 303, the register 301 is clocked to latch in the outputs of the S/P converter 303. Given a bit rate of 10 Gb/sec, the first register 301 is clocked at a rate of 77 MHz. The period of this clock is also referred to herein as a cycle. As such, 128 bits of the input serial data stream D(i) are shifted into the S/P converter 303 and latched into the first register 301 every cycle.

[0030] The first register 301 is coupled to a second register 302, which is also 128 bits wide. During a second cycle, the contents of the first register 301 are latched into the second register 302. As such, the contents of the second register 302 are the same as the contents of the first register 301 one cycle later. In other words, after two cycles, the contents of the second register 302 are D(0)-D(127) and the contents of the first register 301 are D(128)-D(255), where D(0) is the earliest bit of the input serial bit stream.

[0031] A multiplexer 305 is coupled to the registers 301 and 302 so that bit 0 of register 301 and bits 1 through 127 of register 302 are coupled to a first set of 128 inputs of the multiplexer (labeled "ODD") and bits 0 through 127 of register 302 are coupled to a second set of 128 inputs of the multiplexer (labeled "EVEN"). Under the control of a selection signal (ODD/EVEN), the multiplexer 305 provides either the 128 ODD inputs or the 128 EVEN inputs to corresponding outputs of the multiplexer. The 128 outputs of the multiplexer 305 are coupled in parallel to a variable rotator 308."

Applicant submits that none of the references cited by the Examiner, whether taken alone or in combination, teach or suggest claim 10 as amended. Claim 10 and its dependent claims 11-17 are thus allowable.

In view of the foregoing, Applicant believes all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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